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Form 1449*

Atty. Docket No.: 884.141US1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Applicant: Kiran Ganesh et al.

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U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No			
**Examiner Initial		(OTHER DOCUM						
(P)	VLSI Desig	gns", <u>Proc</u>	., "GeneSys: A Lea ceedings of the 12th (Jan. 1999)						
(Pa)		s", <u>Procee</u>	"CLIP: An Optimiz edings of the 34th D						
Pa	Two-Dimens	Gupta, A., et al., "Near-Optimum Hierarchical Layout Synthesis of Two-Dimensional CMOS Cells", <u>Proceedings of the 12th International Conference on VLSI Design</u> , 453-459, (Jan. 1999)							
Æ.	Integer Pi	Gupta, A., et al., "Width Minimization of Two-Dimensional CMOS Cells Using Integer Programming", <u>Proceedings of the IEEE/ACM International Conference on CAD</u> , 660-667, (1996)							
A.C.	Ho, J., et	Ho, J., et al., "New Algorithms for the Rectilinear Steiner Tree Problem", IEEE Transactions on Computer-Aided Design, Vol. 9, 185-193, (Feb. 1990)							
P	Hsieh, Y., Computer-A	Hsieh, Y., et al., "LiB: A CMOS Cell Compiler", IEEE Transactions on Computer-Aided Design, Vol. 10, 994-1005, (Aug. 1991)							
(C)	Proceeding	Hu, C., et al., "Electromigration Under Bidirectional Current Stress", <u>Proceedings of the Symposium on Reliability of Metals in Electronics</u> , 188-202, (1995)							
PP	and Its A	utomatic S	., "An Efficient La Synthesis", <u>IEEE Tra</u> s and Systems, Vol.	nsactions on Co	mputer-Aid	led Design of			
PR	Two-Dimens	sional Dig	., "Transistor Leve gital VLSI Cell Synt Michigan, Ann Arbor,	hesis", <u>Technic</u>	al Report				

Examiner

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**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Sheet 2 of 2

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OTHER DOCUMENTS

**Examiner Initial (Including Author, Title, Date, Pertinent Pages, Etc.)

09/43/47 11/01/99

AN)

Romeo, F., et al., "Research on Simulated Annealing at Berkeley", <u>Proceedings</u> of the IEEE International Conference on Computer Design: VLSI in Computers, 652-657, (Oct. 1984)

(PD)

Saika, S., et al., "A Two-Dimensional Transistor Placement Algorithm for Cell Synthesis and Its Application to Standard Cells", <u>IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E80-A</u>, 1883-1891, (Oct. 1997)

PD

Tani, K., et al., "Two-Dimensional Layout Synthesis for Large-Scale CMOS Circuits", <u>IEEE Internaltional Conference on Computer-Aided Design</u>, 490-493, (Nov. 1991)

Pa

Wimer, S., et al., "Optimal Chaining of CMOS Transistors in a Functional Cell", <u>IEEE Transactions on Computer-Aided Design, Vol. CAD-6</u>, 795-801, (Sept. 1987)

Examiner Shallakes Kik

Date Considered